

# Power MOSFETs

## Reliable MHz Operation Requires Attention to Device Characteristics

Charles Schultz, Vicor Corporation, Andover, Massachusetts

**P**ower MOSFET data sheets do not always present an accurate picture for operation at MHz frequencies, particularly with regard to device capacitance. A recommended approach is to model the full capacitance versus voltage curve as a fitted function and then define an equivalent linear capacitance based on the needs of the application. It is necessary to model the capacitance accurately down to zero drain-to-source voltage and up to the device's rated voltage. In zero current switched (ZCS) converters, output capacitance at very low drain-to-source voltage (near zero) and at high values of drain-to-source voltage can be the defining difference in the suitability of a MOSFET for MHz switching. Circuit simulators can be used for preliminary evaluation purposes, but these still require that the device in question be accurately modeled over the full range of drain-to-source voltages.

Figures of merit used to define MOSFET quality are not always relevant to the designer. For low frequency or nonswitched applications, an appropriate figure of merit may be a resistance times a die area, which essentially eliminates die area by making the figure of merit an effective resistivity. This definition of resistance times die area is also preferred by suppliers since this characterization embodies both performance (resistance) and cost (die area). For high frequency power conversion from hundreds of kHz up to 1MHz, a figure of merit for the MOSFET user will generally include some product of resistance (on-state resistance) times a capacitance. Because the former is inversely proportional to the area

and the latter directly proportional to it, the resulting figure of merit is generally independent of chip area (neglecting inactive silicon area). Thus, figures of merit are functions of the technology and processes used in manufacturing the device.

For switching applications the resistance of interest is of course the  $R_{DS(on)}$  of the MOSFET at some specified condition, but at higher frequencies, device capacitance becomes increasingly more relevant. The capacitance to use in a figure of merit will depend entirely on the application. This capacitance may be the input capacitance  $C_{iss}$ , the output capacitance  $C_{oss}$ , the Miller capacitance  $C_{rss}$ , or some equivalent capacitance that more accurately characterizes how the device will work in a circuit. An example of an equivalent capacitance appropriate to a figure of merit is one derived from the total gate charge (e.g.,  $Q_t/10V$ ). Furthermore, the capacitance of a MOSFET is highly non-linear versus drain-to-source bias voltage, so in evaluating a device there is the additional question of which drain-to-source voltage is most appropriate for the capacitance.

Generally the value of capacitance at 25V is specified in data sheets but this is inadequate for analyzing high frequency MOSFET switching. Typical curves are often provided as a function of applied drain-to-source voltage, but rarely do they extend down to zero bias or conversely up to the device's rated voltage (in the case of higher voltage devices).

### ZCS Example

Consider the resonant-mode zero current switched (ZCS) dc-dc power converter<sup>[1]</sup> indicated in *Fig-*

**Operating power MOSFETs consistently and reliably in the MHz region requires a careful evaluation of the effect of its circuit capacitance and special analytical techniques for an accurate determination of device performance.**

ure 1. For brevity the control circuit is not shown but employs variable frequency control. The power MOSFET switch is turned off once the primary resonant current returns to zero. The input voltage range is 200 to 400Vdc, with an output of 5V at 200W. The topology is single-ended forward using a low-side MOSFET switch.

Figure 2 is an example of a typical drain waveform in arbitrary units at an arbitrary line/load condition. At turn-on, the drain voltage is pulled down to within an  $R_{DS(on)}$  drop of the input return. At turn-off, the voltage increases to a value  $V_f$  consistent with resetting the core of T1.

Energy stored in the MOSFET's output capacitance must be removed to turn the device fully on. Because the MOSFET's capacitance is essentially a junction capacitance, it is highly nonlinear and depends on the instantaneous drain-to-source voltage. In the absence of zero voltage switching (ZVS), the MOSFET's output capacitance  $C_{oss}$  must be discharged from the peak drain voltage during T1 reset to an  $R_{DS(on)}$  voltage drop. This energy is generally dissipated as heat in the silicon. Hence, the average power dissipation at turn-on equals the energy removed from  $C_{oss}$  times the switching frequency. Next, consider turn-off in the circuit of Figure 1. The transformer's load current has returned to zero allowing turn-off to be affected at essentially zero current (ZCS). The current necessary to recharge the MOSFET output capacitance is extracted from the magnetizing energy stored in transformer T1. This current must be sufficient to turn off the device in a reasonable amount of time. For example, switching up to a 1MHz rate will generally require that the total delay plus rise time at MOSFET turn-off be no greater than about 200nsec. Turn-off in this application, under true ZCS conditions, is limited by magnetizing current rather than the ability of the drive circuit to sink gate current.

The two examples above illustrate

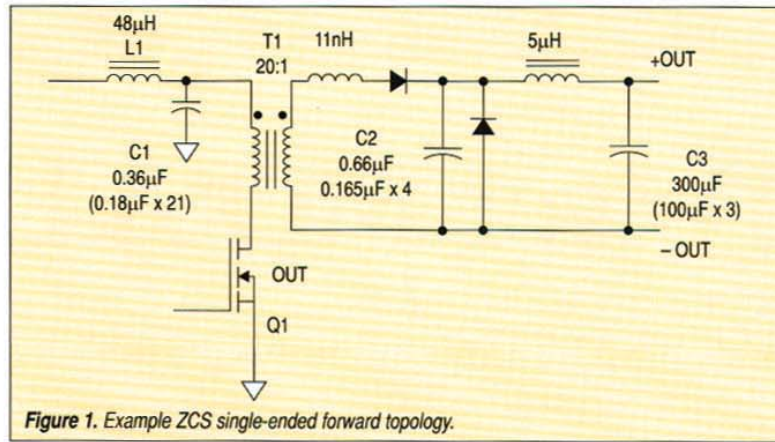


Figure 1. Example ZCS single-ended forward topology.

the relevance of the total output capacitance curve. At turn-on, switch loss is proportional to the energy discharged from the nonlinear output capacitance as its drain-to-source-voltage drops to essentially zero (an  $R_{DS}$  drop). At turn-off, the rise time of the switch is driven by the magnetizing current. Thus, output capacitance  $C_{oss}$  in this application affects switching loss at turn-on and determines the MOSFET rise time at turn-off. Because the drain-to-source voltage is traversing a wide voltage swing in either case, the full capacitance curve must be accounted for. A typical output capacitance for a 600V MOSFET is indicated in Figure 3 – illustrating in particular the high value at zero drain-to-source bias. Thus, returning to the above discussion of figures of merit, the full capacitance curve is relevant and in fact the value of capacitance down at zero drain-to-source bias is significant, particularly at turn-off. At the beginning portion of the turn-off cycle, the high value of output capacitance (low drain-to-source voltage) will increase the effective turn-off delay over and above any delay introduced by the gate circuit.

### Calculating Losses

The primary load current at turn-on in the isolated single-ended forward converter is initially zero. The main contributor to switching loss is the energy stored in the MOSFET's

output capacitance. For higher voltage MOSFETs (>400V rated), switching losses will approach conduction losses as frequencies approach a MHz. One-half times the capacitance times the square of the voltage is satisfactory for linear capacitors but not appropriate in this example. To develop a useful and accurate algorithm to handle this scenario, a mathematical model for MOSFET output capacitance ( $C_{oss}$ ) is required. Junction capacitance is generally represented by an inverse power law. Of course any well-behaved function can be fit to a power series (or inverse power series) if enough terms are used. Experience shows that for most MOSFETs, a good fit is provided by the well-established inverse power law (with coefficients  $C_{jo}$ ,  $n$ ,  $V_j$ ) plus a constant capacitance  $C_{off}$ :

(1)

$$C_{oss}(V) = C_{off} + \frac{C_{jo}}{\left(1 + \frac{V}{V_j}\right)^n}$$

where:

$C_{jo}$ ,  $n$ ,  $V_j$  and  $C_{off}$  = Constants  
 $V$  = Applied voltage across the device

The constant term is a linear capacitance and may represent a package capacitance. In general however, it is a term that improves the functional fit. To calculate the energy lost in the turn-on transition, the energy integral

must be solved:

$$E_{SW} = \int_0^{V_r} C_{oss}(V) \times VdV \quad (2)$$

where:

$V_r$  = Initial drain-to-source voltage at turn-on

Substitution of Equation (1) into Equation (2) yields the following expression for switching loss at turn-on:

$$E_{SW} = \frac{1}{2} C_{eff1} V_r^2 \quad (3)$$

where:

$$C_{eff1} = \frac{2C_{jo} V_j}{V_r(1-n)} \left[ 1 + \frac{V_r}{V_j} \right]^{(1-n)} \quad (4)$$

$$- \frac{2C_{jo} V_j^2 \left[ \left( 1 + \frac{V_r}{V_j} \right)^{(2-n)} - 1 \right]}{V_r^2 (1-n)(2-n)} + C_{off}$$

The value  $C_{eff1}$  is therefore an effective linear (constant) capacitance which, when charged or discharged to a voltage  $V_r$ , results in the same amount of energy transfer as the MOSFET's actual nonlinear output capacitance. In the application above near 1MHz, this effective capacitance is necessary to determine accurately this component of switching loss. Because most of the energy storage on a MOSFET is done at higher voltages, the capacitance at high drain-to-source voltages (near  $V_r$ ) weighs more heavily into  $C_{eff1}$ . In single-ended forward converters, switching losses at turn-on may be minimized, and in some instances (e.g., ZCS) essentially eliminated, by using an appropriately timed active reset circuit and exploiting magnetizing current reversal to losslessly discharge the switch and circuit parasitic capacitances<sup>12</sup>.

## Rise Time

Consider MOSFET turn-off in *Figure 1*. Load current is zero by design (ZCS) leaving the magnetizing current alone to charge the nonlinear output capacitance. Other elements in

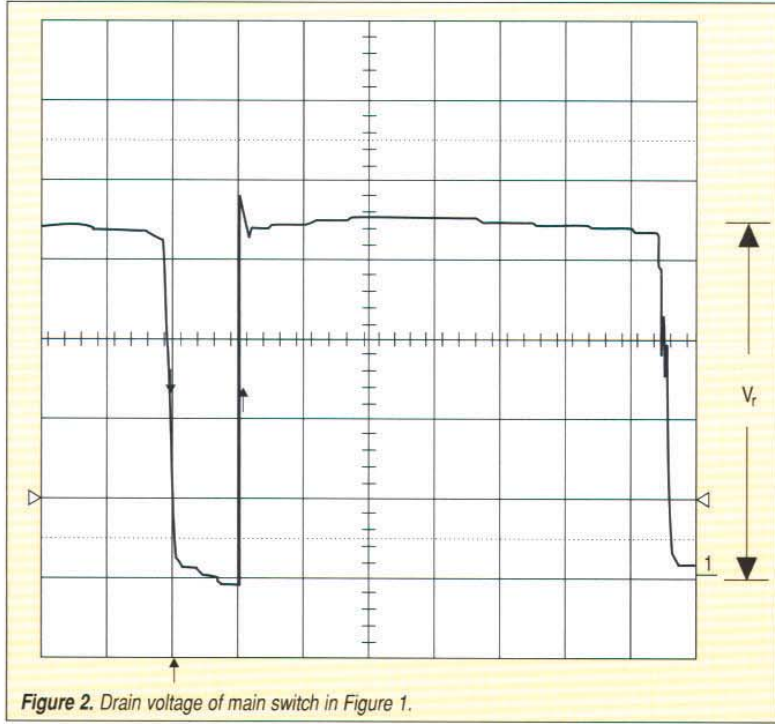


Figure 2. Drain voltage of main switch in Figure 1.

the circuit (reflected rectifier junction capacitance, transformer winding capacitance, parasitic board capacitance, etc.) must be charged up as well, but these will be neglected here for simplicity. Once the MOSFET gate is driven down to its plateau voltage (threshold voltage under magnetizing load), the voltage across it will begin to rise. For relatively fast rise times, the magnetizing current in the transformer primary winding will be constant and equal to its peak value at the end of the switch conduction interval. Assuming the application is such that the gate driver can sink much more current than is available to recharge  $C_{oss}$ , turn-off time is driven by charge transfer to the nonlinear MOSFET output capacitance  $C_{oss}$ .

The amount of charge required to drive the MOSFET output capacitance to a drain reset voltage  $V_r$  is determined by the charge integral.

$$Q_{SW} = \int_0^{V_r} C_{oss}(V) dV \quad (5)$$

Rise time can then be calculated based on:

$$\tau_{rise} = \frac{Q_{SW}}{I_m} \quad (6)$$

where:

$I_m$  = Peak magnetizing current

The peak magnetizing current,  $I_m$ , occurs at the end of the MOSFET's conduction interval. Substituting Equation (1) into Equation (5) and then into Equation (6) yields:

$$\tau_{rise} = \frac{C_{eff2} \times V_r}{I_m} \quad (7)$$

where:

$$C_{eff2} = \frac{C_{jo} V_j \left[ \left( 1 + \frac{V_r}{V_j} \right)^{(1-n)} - 1 \right]}{V_r (1-n)} \quad (8)$$

$$+ C_{off}$$

The value  $C_{eff2}$  is therefore an effective linear (constant) capacitance which, when charged or discharged to a voltage  $V_r$ , results in the same amount of charge transfer as the MOSFET's actual nonlinear output capacitance. In applications where rise time

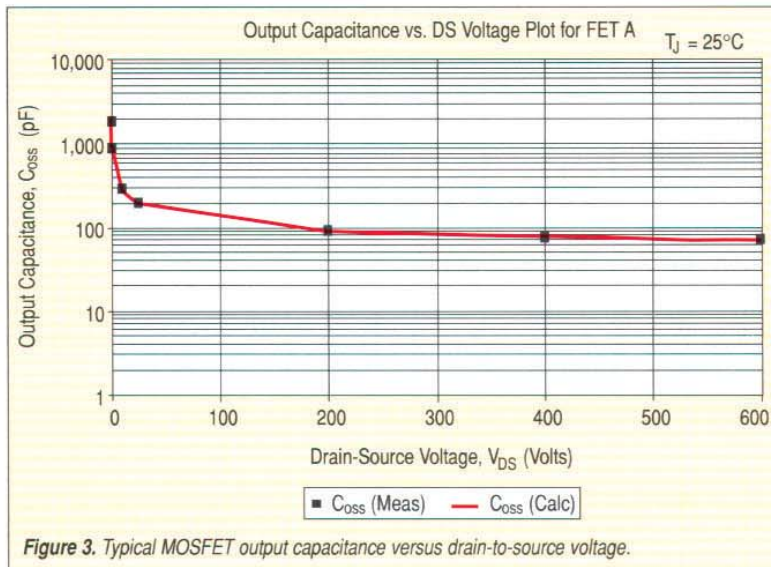


Figure 3. Typical MOSFET output capacitance versus drain-to-source voltage.

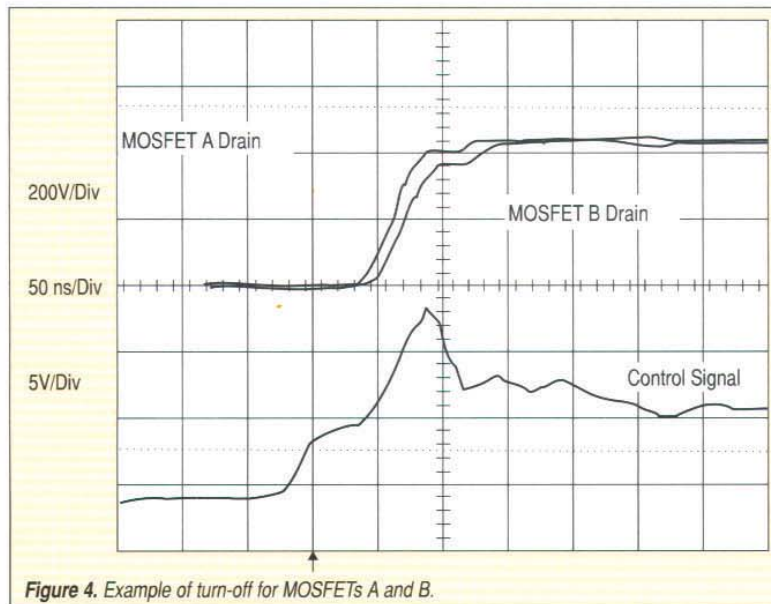


Figure 4. Example of turn-off for MOSFETs A and B.

is limited by available drain current, Equation (8) would be needed to accurately predict rise time. In actual circuit operation, other capacitances, which equivalently would appear from drain-to-source of Figure 1, should be taken into account to accurately predict rise time. Because most of the charge transfer is done at low drain-to-source voltages, the value of output capacitance near zero bias weighs more heavily into Equation (8). This is in contrast to the equivalent capacitance defined by the energy integral whereby output capacitance near  $V_f$  contributes more significantly to ener-

gy storage. A high output capacitance at zero bias in this instance will cause an additional delay time (measured by the 10% point) in the MOSFET voltage relative to the controller off signal. In the case of the energy integral and the charge integral, the output capacitance near 25V as commonly found in data sheets is not the most relevant.

Calculation of rise time is by no means insignificant for operation near 1MHz in ZCS designs and can in fact result in significant stretching of the MOSFET's duty cycle (versus the controller's duty cycle). This stretching results in higher peak voltage

stress on the switch and increases power loss in the transformer (higher core loss).

Figure 4 shows an example of two MOSFETs in the same physical circuit illustrating the difference in turn-off behavior. The top waveform is the superimposed drain signal of each device (200V/div) at turn-off. The bottom waveform represents a common control signal initiating the turn-off. MOSFET A (Figure 3) is characterized by:

$$n = 1.02974$$

$$C_{jo} = 2177.108\text{pF}$$

$$V_j = 1.655\text{V}$$

$$C_{off}^j = 33\text{pF}$$

The effective output capacitance,  $C_{eff}^{j2}$ , for recharging to a final voltage  $V_f$  of 440V is 75.4pF. MOSFET B is a slightly larger device characterized by:

$$n = 1.4037$$

$$C_{jo} = 2711.73\text{pF}$$

$$V_j = 3.2898\text{V}$$

$$C_{off}^j = 45.7\text{pF}$$

Its effective capacitance,  $C_{eff}^{j2}$ , to 440V calculates to 89.0pF. The higher effective output capacitance of device B increases its turn-off time. More significant differences in die size and/or output capacitance versus the devices in Figure 4 leads to even more pronounced differences in turn-off times.

## References

1. P. Vinciarelli, "Forward Converter Switched at Zero Current," U.S. Patent 4,415,959.
2. P. Vinciarelli, "Optimal Resetting of the Transformer's Core in Single Ended Forward Converters," U.S. Patent 4,441,146 and subsequent reissues.



## Component Solutions For Your Power System

25 Frontage Road  
Andover, MA 01810  
Tel: 978 470 2900  
Fax: 978 475 6715  
www.vicr.com

PN 20969