



# PAC

## Phased Array Controller

Part number 19077

### Features

- Enhances performance of parallel converter arrays
- Reduces peak reflected input ripple current and output ripple voltage
- Multi module control in a single SOIC package
- Autoconfigures for up to twelve modules
- Internal watchdog circuit for fault detection

### Description

The Phased Array Controller (PAC) integrated circuit enhances the performance of large power sharing arrays of modular DC-DC converters. This device is intended for processing load share signals on the parallel bus of Vicor Maxi, Mini, Micro Series converters. Utilization of the PAC forces equal separation in time of power conversion pulses produced by each module in the array, thereby substantially reducing the peak magnitude of input reflected ripple current and output ripple voltage. Input and output filter requirements are reduced accordingly, yielding a significant impact on cost and complexity of the overall power conversion system.

### Absolute Maximum Ratings

V<sub>CC</sub> ..... - 0.3 V to + 6 V  
 PC Inputs ..... - 0.3 V to V<sub>CC</sub> + 0.3 V  
 PR Inputs ..... - 0.3 V to V<sub>CC</sub> + 0.3 V  
 Operating Temperature Range ..... -40 to + 85°C  
 Storage Temperature Range ..... - 65°C to + 150°C  
 Lead Temperature (soldering, 10 secs) ..... + 300°C  
 Power Dissipation to + 75°C ..... 1000 mW  
 Derates above + 75°C by ..... 10 mW/°C

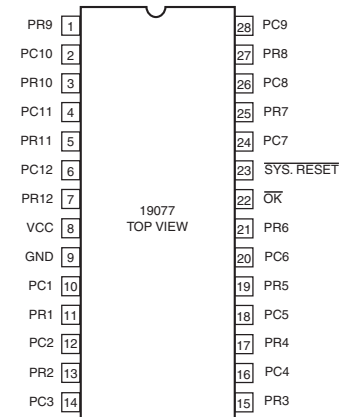


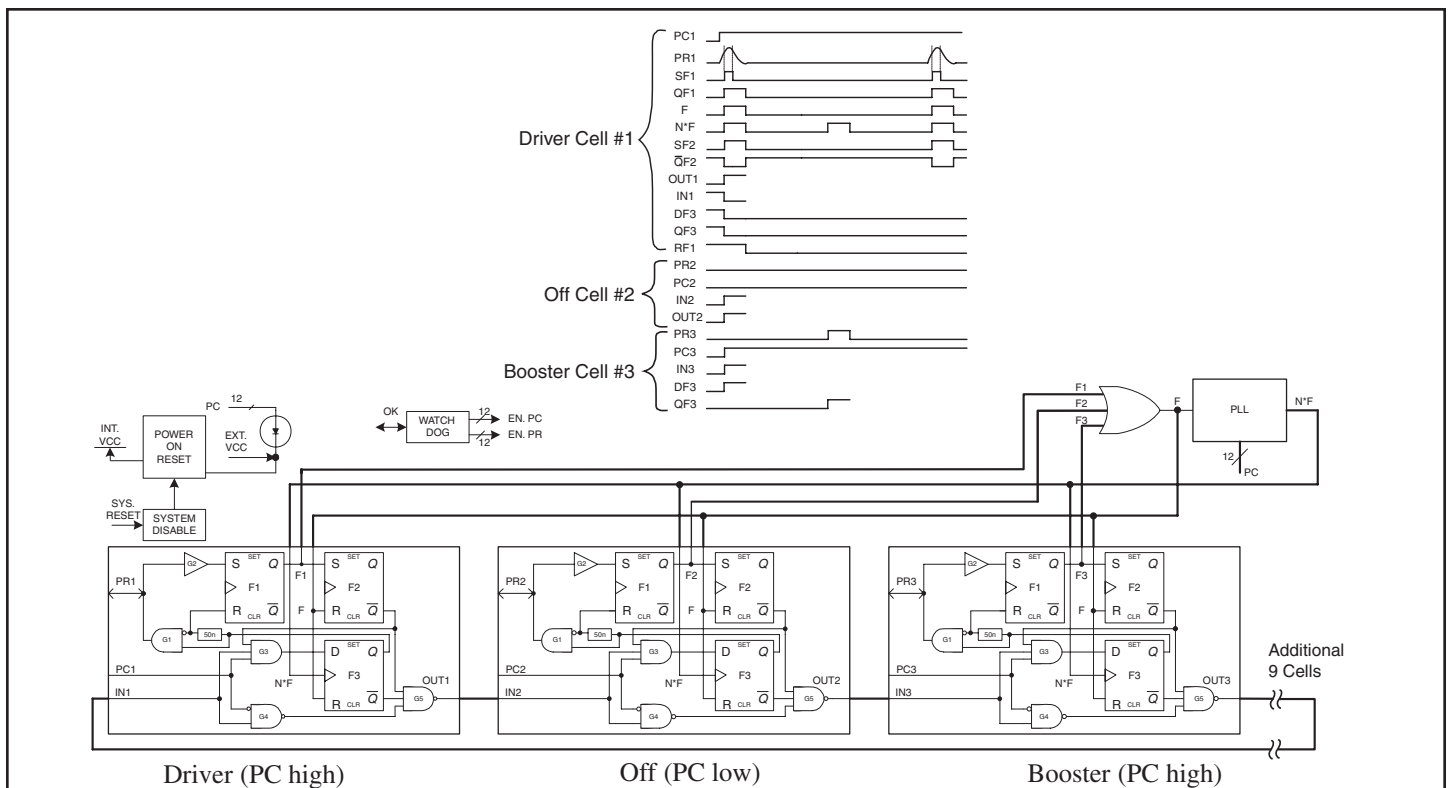
Figure 1—SOIC Package

### ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub>=5.0 V, T<sub>A</sub>=+25°C, R<sub>L</sub>=350Ω, C<sub>L</sub>=50 pF, unless otherwise noted.)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V <sub>PCIH</sub>	PC Positive Going Threshold	2.7	3.0	3.2	V	
V <sub>PCIL</sub>	PC Negative Going Threshold	2.2	2.5	2.7	V	
I <sub>PC</sub>	PC Input Current		1.0	1.5	mA	With no external V <sub>CC</sub> supply
I <sub>CC</sub>	V <sub>CC</sub> Current			15.0	mA	12 modules-each operating at 1 mhz
V <sub>PRIH</sub>	PR Positive Going Threshold	2.7	3.0	3.2	V	
V <sub>PRIL</sub>	PR Negative Going Threshold	1.5	1.7	2.0	V	
V <sub>PROH</sub>	PR Output High Voltage		4.2 4.7		V V	V <sub>CC</sub> =5.0 V @ I <sub>PROH</sub> =12.1 mA V <sub>CC</sub> =5.5 V @ I <sub>PROH</sub> =13.5 mA
V <sub>PROL</sub>	PR Output Low Voltage		0 0		V V	V <sub>CC</sub> =5.0 V @ I <sub>PROL</sub> =0.0 mA V <sub>CC</sub> =5.5 V @ I <sub>PROL</sub> =0.0 mA
V <sub>SRIH</sub>	SR POSITIVE GOING THRESHOLD	2.2	2.5	2.8	V	
V <sub>SRIL</sub>	SR Negative GOING THRESHOLD	1.9	2.2	2.4	V	
f <sub>PR</sub>	PR Frequency	20		1000	kHz	
T <sub>WPR</sub>	PR Width	40	45	50	ns	
Timing ERROR	PR Driver to Booster Error		±.05T+20 max		ns	See Note 1
Timing ERROR	PR Booster to Booster Error		±.01T+5 max		ns	See Note 1
	PR Jitter			0.05	%	
	Lock Up Time			100	Cycles	MAX 500μSec

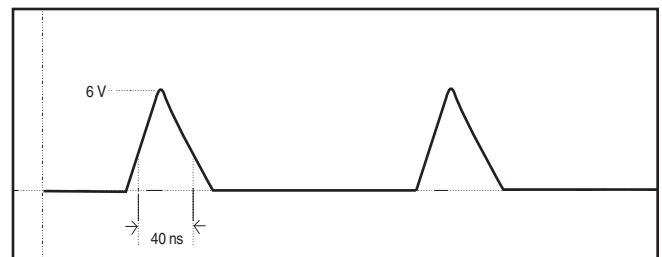
Note 1: T is period of driver PR divided by N. Where N is the number of PC pins driven high.



**Figure 2**—Simplified functional block and timing diagrams illustrating three operational cells, where cell #1 interfaces the driver module, cell #2 interfaces a disabled module, and cell #3 interfaces a module operating in the booster mode.

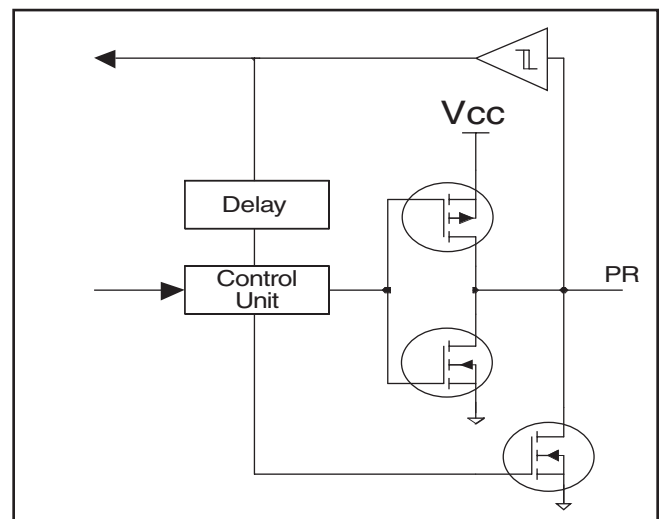
## PIN FUNCTION DESCRIPTIONS

**PR 1-12 (PARALLEL):** The Parallel (PR) pin is a bi-directional port. As an input, the PR pin of the PAC receives sync pulse information from the module which is controlling the array. As an output, the Parallel pin provides phase displaced synchronous information to the slave modules. The frequency of the PR signal is variable and is used to trigger the power pulse transfer from the primary to the secondary of the transformer within each converter.



**Figure 3:** Module PR Pulse

The PAC PR pin is active high / low, and is not tri-stated when receiving the driver pulse. At start up, since more than one converter may deliver a sync pulse, each PR pin listens to it's module. The PR pulse is received from a low impedance emitter follower within a converter. As shown in figure 3, the typical wave-shape is a triangular pulse. Figure 4 provides a simplified circuit diagram of each PR port within the PAC. As an input, the PAC employs Schmitt triggers to shape incoming PR pulses. Hysteresis provides noise immunity. As an output, the PR signal is generated via a PMOS Driver. Once the driver pulse rises above the Schmitt trigger threshold, the Schmitt will send a signal to the control circuitry that is delayed by approximately 50 ns(typ). After the delay time, the control circuitry will send a signal to turn on an NMOS pull down transistor, which has low channel impedance, thus terminating the pulse.

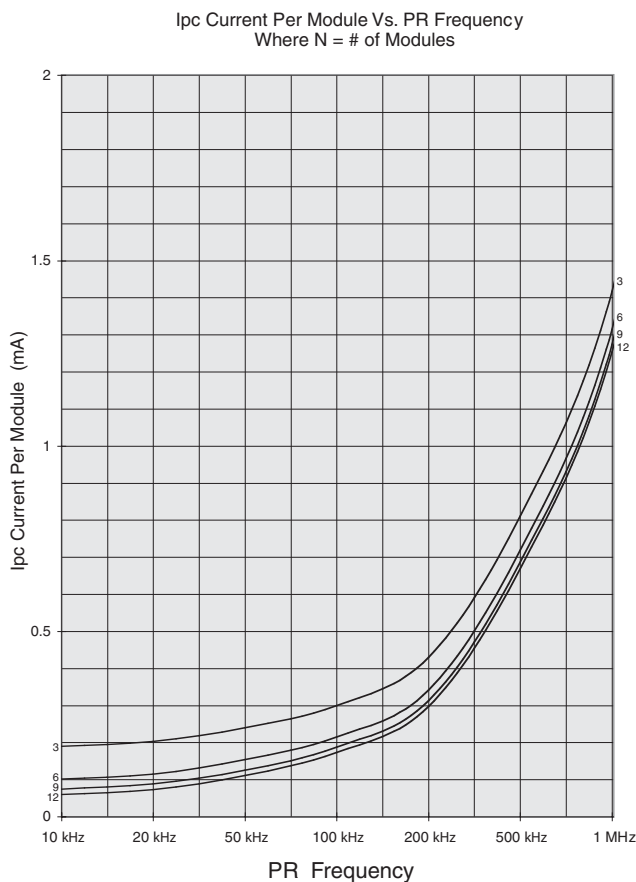


**Figure 4:** PR In/Out port

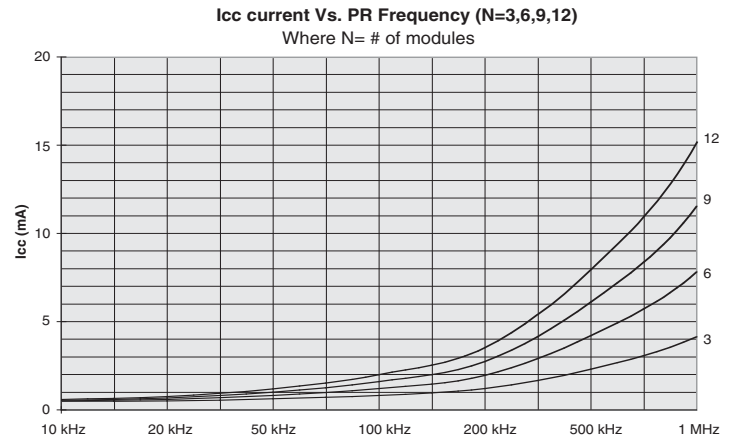
**PC 1-12 (PRIMARY CONTROL):** The Primary Control (PC) pin is also a bidirectional port. In addition to communicating module status information, the PAC can receive power from a module array's PC pins, eliminating the need for a separate external 5 V power supply referenced to the primary side of the converters. The PAC may require up to 1.5 mA supply current per operating module depending on operating frequency, as illustrated in figures 5a, 5b, and 5c. In all configurations, the PC pin is also used as a logic input to inform the PAC that a converter module is operating on the corresponding channel. When the interfaced converter is operating properly, PC assumes the high state. If a fault occurs within a converter, it's PC pin goes low, the module is shutoff, and the PAC is notified. The PAC responds by reconfiguring the sync pulse decoding logic in order to adjust the sync pulse sequence. The voltage on the PC pin delivered by the module is 5.9 V +/- 200 mV during normal operation. The low, or fault state PC voltage is less than 0.5 V. While the

SYSTEM RESET input of the PAC is held low, the PC pin is driven low with active pull down and will sink the maximum current available from the associated converter. The PAC internal circuitry receives current from all PC pins via a diode "OR" of all PC signals, which serves as internal Vcc. Similar to the PR pins, the PAC's PC pins utilize Schmitt triggers for noise immunity.

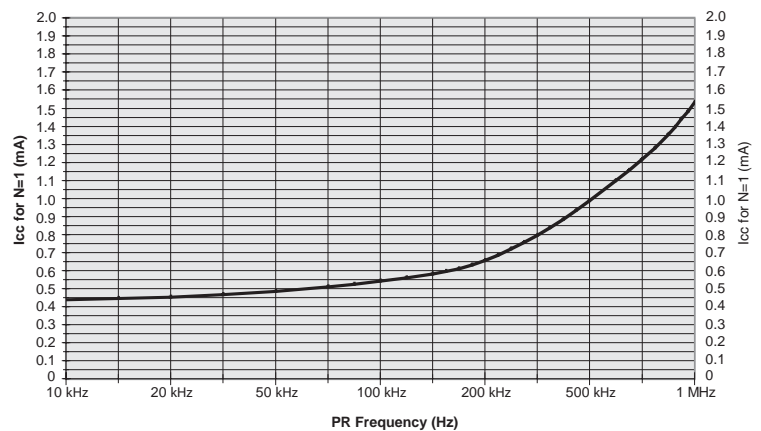
**OK:** The OK pin is a multifunction I/O pin used as a flag signal to indicate normal or abnormal operation, and to reset the PAC chip after a fault is detected. It's normal active low state is achieved with a driver capable of sinking 5 mA (to illuminate a green LED, for example). During a fault, OK is in the high state with internal pull up limited to 5  $\mu$ A. When the fault is detected, the internal latch can be reset by forcing the OK pin low via an external switch. Similar in nature to the PR pin, the OK pin employs Schmitt triggers as buffers.



**Figure 5a:** Ipc current per module vs. PR frequency Where N = # of modules



**Figure 5b:** Icc current Vs. PR Frequency (N=3,6,9,12 modules)



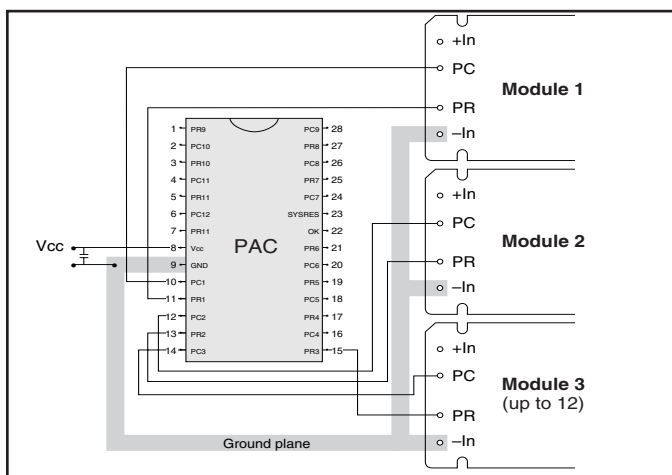
**Figure 5c:** Average current Icc for N=1 Vs. PR frequency

**System\_Reset:** The RESET pin is an input pin used to disable the PAC chip. The system reset also disables the array by pulling all PC pins low and commanding all PR pins to assume the high impedance state. The minimum pulse width required for detection is 1  $\mu$ sec. The PAC responds asynchronously to the input falling edge, disabling the internal circuitry of the PAC but not Vcc. The System Reset employs a Schmitt trigger as an input buffer.

**Vcc:** The Vcc pin provides an alternate means to power to the PAC. Alternatively, power may be provided via the PC pins, which are diode OR'd to the internal Vcc node. Vcc is the internal supply voltage of the PAC IC. This is wire-bonded to two pads on the IC, called Vccl (for the logic) and Vccd (for the drivers). The separate conductors prevent the high Ldi/dt in the driver stages from disturbing the analog & digital circuitry in the core. In any configuration, power may be provided by the external Vcc pin. The external supply must be capable of supplying 5.0+/-0.5 V@1.5\*NmA, where N is the number of converter modules in the array.

## APPLICATIONS INFORMATION

One advantage of the Vicor converter topology is that these variable frequency, quasi-resonant, zero current switching DC-DC converter modules lend themselves to a novel load share scheme based on frequency synchronization. This method is uniquely compatible with the variable frequency topology, where line and load regulation is accomplished by controlling the frequency, or rate at which pulses of energy are transferred from the primary to the secondary of the isolation transformer. The pulse width, and therefore the energy per pulse is constant at any given input voltage. The pulse repetition rate is therefore representative of output power, and is controlled to maintain output voltage regulation while satisfying the load current demand.

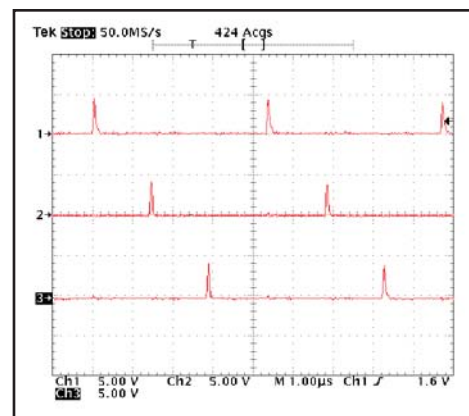


**Figure 6:** Interconnection of the PAC chip with three Vicor Maxi, Mini, Micro Series DC-DC converters.

It follows therefore that identical converters in a parallel array will inherently share the load if the switching frequencies are synchronized. The switching frequency vs line / load characteristic is uniform to within 5% among modules of a given type. The PR (parallel) pin on Vicor Maxi, Mini, Micro Series converter modules is a bidirectional port which serves as a parallel load share bus. This port can transmit or receive the synchronizing pulse signal which is coincident with the leading edge of the internal power conversion pulse. The controlling module transmits the sync pulse while all other modules listen. These converters also possess the ability to self arbitrate the leadership role. One module always assumes command of the entire array. If this module experiences a fault condition, another will take over. The PC pin, which is normally high (6 V) during operation, switches low in the event that the module shuts down and periodically toggles high as an attempt to restart. Transfer of the leadership role is completely transparent, i.e., the output power bus is virtually unaffected by the transfer process. This feature is particularly useful in parallel arrays that employ redundancy for fault tolerance.

By contrast, the pulsed synchronous current share scheme offers considerable advantages over commonly used analog methods, which require either an artificial increase of the output source impedance of each converter, or a current sense device at the output of each converter. When using the Phased Array Controller (PAC), sync pulse processing produces a sequential and equal distribution of the power conversion pulses generated by each module in the array. This in turn eliminates the coherent summation of conducted and radiated EMI that is associated with the usual coincident occurrence of energy conversion pulses.

The PAC is able to support up to twelve DC-DC converter modules and has dedicated input / output ports for



**Figure 7:** The PAC chip supports current sharing and adjusts the relative phase of each module in the array in increments of  $360^\circ/N$ , where N is the number of enabled modules within the array.

communication with both PR and PC pins of each module, as illustrated in figure 6. A multiplying phase locked loop captures and locks on the PR signal from the one converter in the array that operates at the highest frequency to satisfy control equilibrium. Randomly selected modules of a given type typically display less than 5% variance in operating frequencies at any given line / load condition. This is due to internal component tolerances. Decoding logic sequentially provides sync pulses to PR pins of all other modules in the array whose PC pins are high.

The PAC takes full advantage of the ability of Vicor converters to share the load when the operating frequencies are synchronous. The PAC however, provides an additional benefit: phase shifted, frequency synchronous operation. That is, the sync pulses are sequentially generated with respect to the controlling converter, and delivered individually to each converter in the array, so that each generates a power conversion pulse equidistantly displaced in time, rather than simultaneously. Figure 7 illustrates a typical PR pulse sequence for a three module array. The apparent switching frequency of the array is increased by a factor of N, where N is the number of converters in the array. More significantly, the array produces energy conversion pulses of magnitude E, as opposed to NE, which is the case when all switching occurs simultaneously.

There exists a linear relationship between the apparent magnitude of a power conversion pulse produced by the array, the peak reflected input ripple current and the output ripple voltage. Performance tests of converter arrays

employing a PAC have demonstrated a substantial reduction in magnitude of input ripple current, not only of the fundamental switching frequency component  $f$ , but also of all harmonic components generated by individual converters in the array. Equiangular phasor rotation from module to module produces a cancellation effect, as illustrated in figure 8. The conducted emissions spectrum produced by an array where the PAC is employed includes components at  $Nf$  and its harmonics; each carrying upper and lower sidebands at  $f$  and its harmonics. This effect is illustrated in figure 9 for the case of an eight module array. The resulting redistribution of energy over a broadened and upward shifted spectrum substantially reduces the input filter required to meet conducted EMI standards. This is evident in the measurement data presented in figure 10, which illustrates the reflected input current spectrum of an array comprising eight 300 Vin to 5 Vout, 400 W converters delivering 500 Amperes. This array employs only a single 260  $\mu$ H, 40 Ampere common mode choke on the input bus, yet the conducted emissions are under the Class B limit per FCC part 15 and EN55022, with substantial margin.

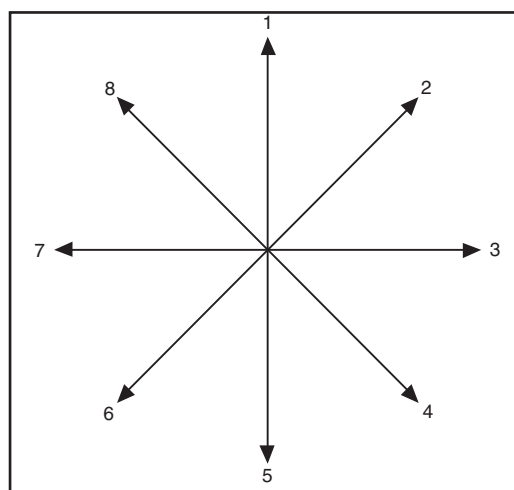


Figure 8: Vector representation of inter module phase rotation; 8-module array with PAC

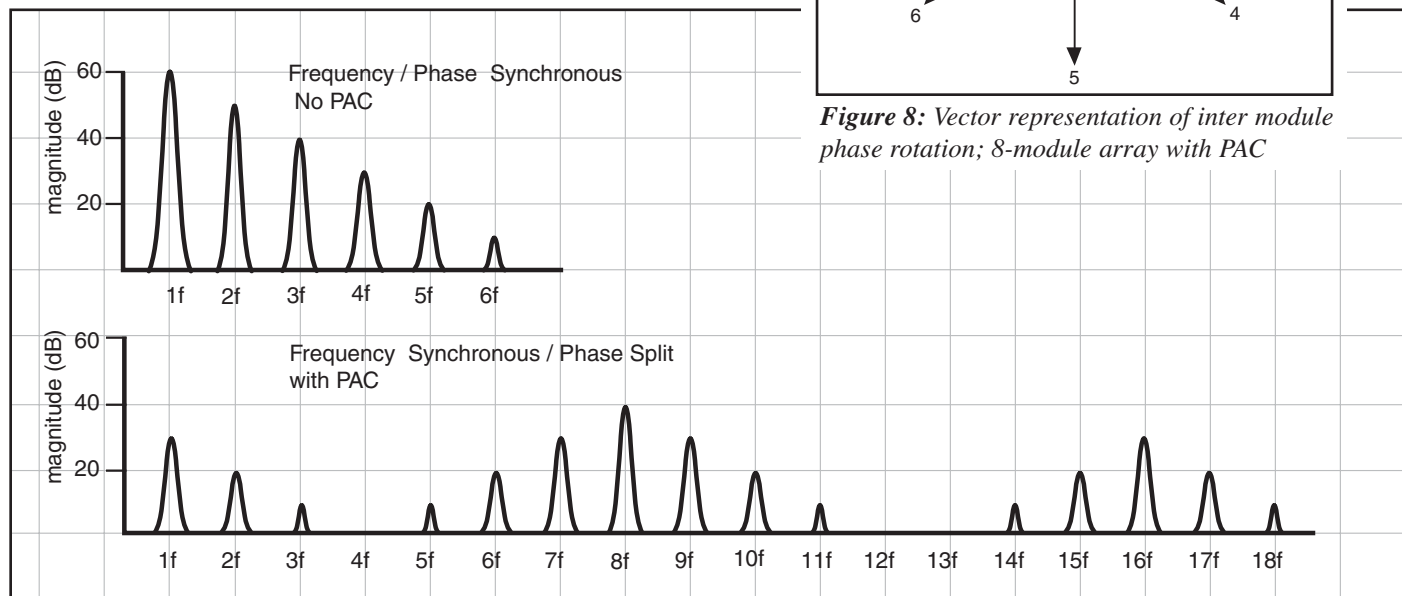


Figure 9: Conducted emissions spectrum of an 8-converter array without PAC, with PAC

## PARALLEL ARRAY DESIGN CONSIDERATIONS

Care must be taken to avoid introducing interfering signals onto the parallel bus as this may prevent synchronous operation and proper load sharing between modules. One possible source of interference is input ripple current conducted via the plus and minus input power pins. The PR signal and DC power input share a common return which is the negative input pin. Steps should be taken to de-couple AC components of input current from the parallel bus. The input to each converter (designated as + and - pins on the input side of the module) should be bypassed locally with a 0.2  $\mu\text{F}$  ceramic or film capacitor. This provides a shunt path for input ripple current. A Y-rated capacitor should be connected between the negative input pin and baseplate of each module, thus creating a shunt path for common mode components of current. Attention to the PC board artwork should minimize the parasitic impedance between negative input pins of parallel modules to insure that all PR pins are referenced to the same potential. Modules should be placed physically close to each other and wide copper traces (0.75in., 2oz. copper) should be used to connect power input pins. A dedicated layer of copper is the ideal solution.

Some applications require physical separation of paralleled modules on different boards, and/or input power from separate sources. In these cases, transformer coupling of the PR signal is required to prevent inter-module common mode “bounce” from interfering with the sync pulse transmission. High speed buffering may be required if the distance between modules is greater than a few inches. All modules, except the one that’s talking, are in the listening mode. Each listener presents a load which is approximately 500 ohms shunted by 30 pF capacitance. Long leads for the interconnection introduce losses and parasitic reactance on the bus which can attenuate and distort the sync pulse signal. The bandwidth of the bus must be at least 60 MHz and the signal attenuation less than 2 dB. In most cases transformer coupling without buffering is adequate. A transformer is available (Vicor P/N 22400) for parallel bus interface that provides SELV isolation and 3000 Vrms dielectric withstand between windings. This transformer (Figure 11) is trifiler wound, 1:1:1 turns ratio. One winding is used, as illustrated in Figure 12 for connection to the module, and another winding provides the isolated bus interface to the PAC. Again, careful attention must be given to layout considerations. Please consult with Applications Engineering at any Vicor Technical Support Center (800-927-9474) for additional information.

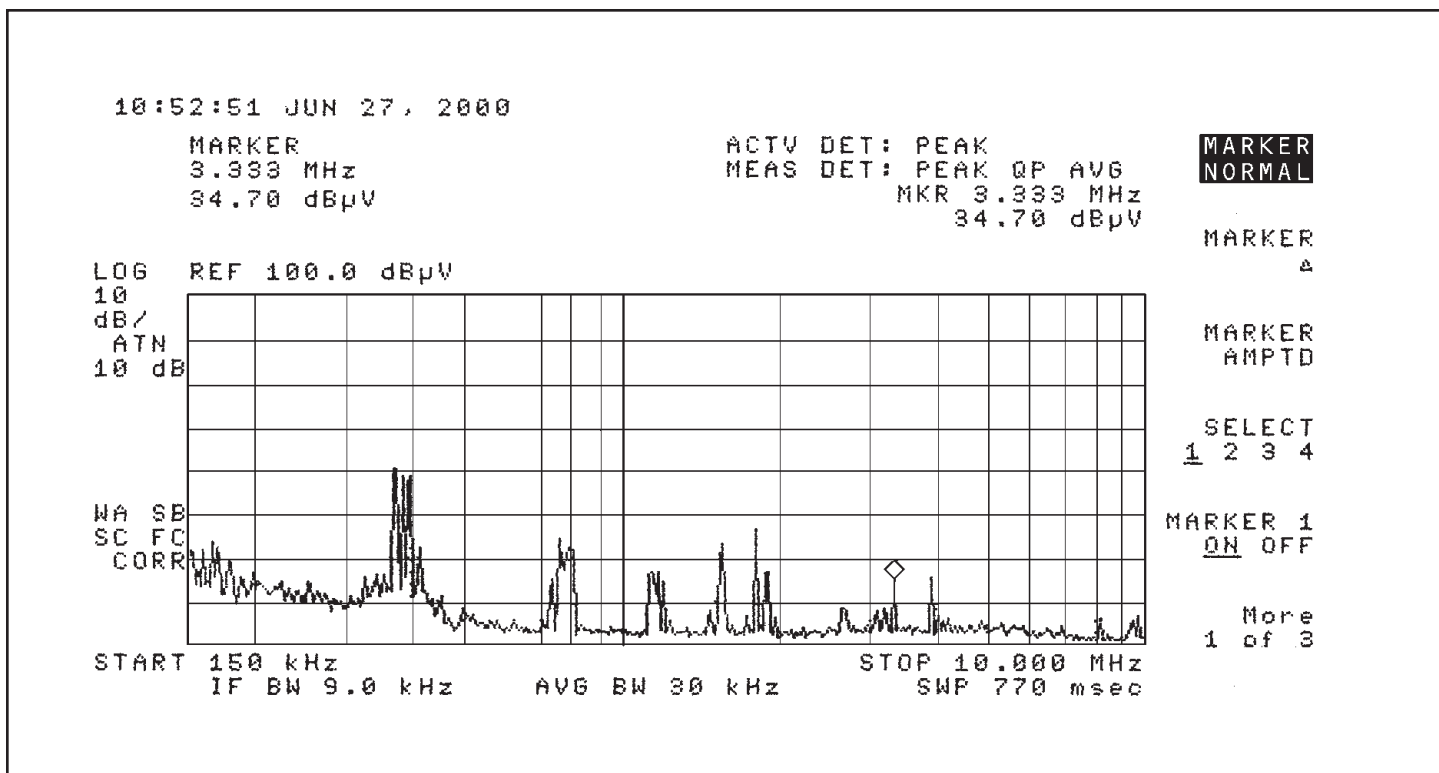


Figure 10: Conducted Emission Spectrum eight module array delivering 5 V, 500 A.

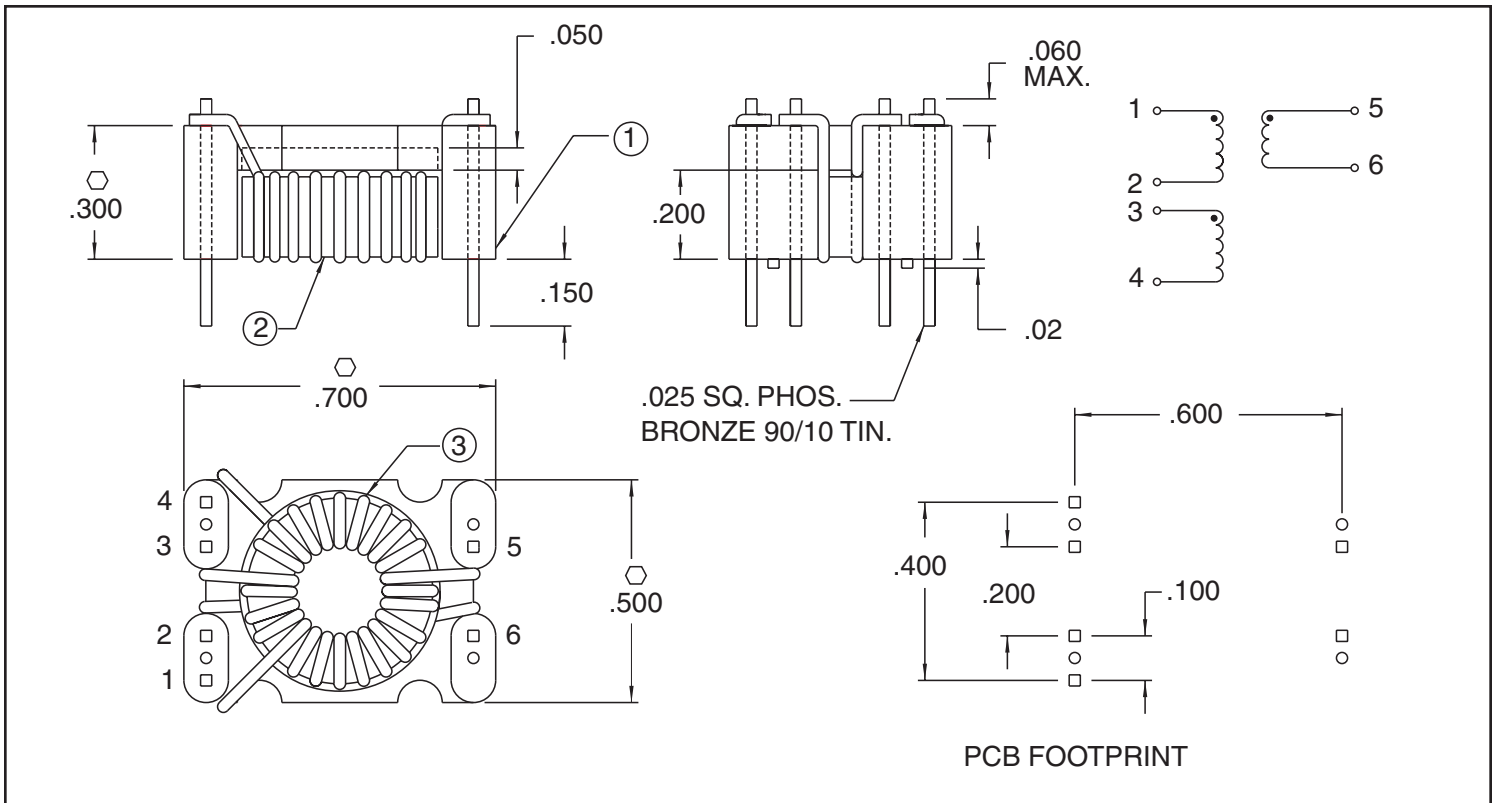


Figure 11: PR Bus Isolation Transformer, p/n 22400

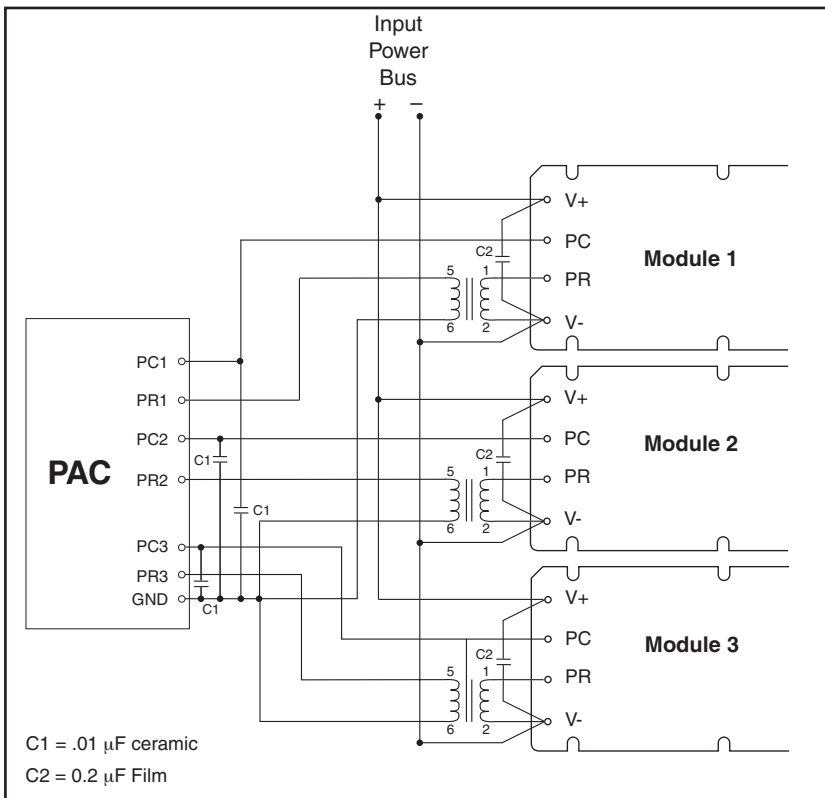


Figure 12: Transformer Coupled PR Bus

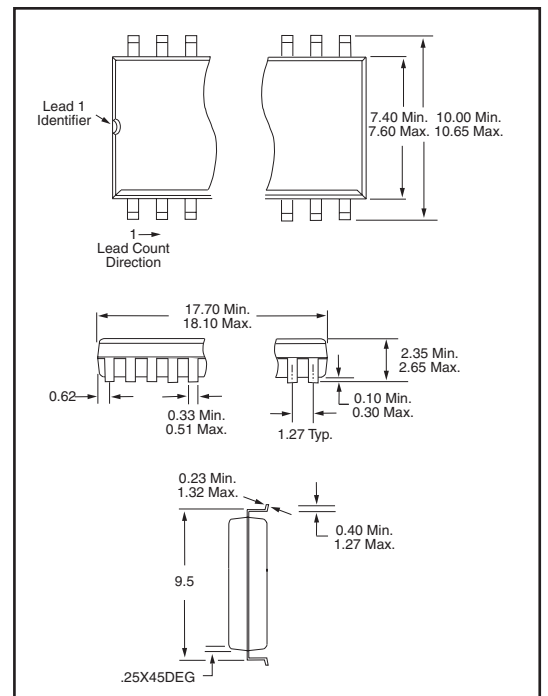


Figure 13: Mechanical Outline

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